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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,790	BANNING ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/1/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 46-53, 61-63 and 66-74 rejected under 35 U.S.C. 102(b) as being anticipated by Tsusihma (patent No. 6,044,450).

Tsushima taught the invention substantially as claimed including a data processing ("DP") system comprising (e.g., see fig. 1): (as per claim 46) a method of executing a processor instruction said method comprising: fetching from memory a first machine language instruction comprising an instruction segment (e.g., see col. 6, lines 1-9); responsive to a trigger pattern(group code fields 10A,16 in figs. 2C and 2D) in said first machine language instruction, modifying said instruction segment to form a second machine language instruction; and executing on said processor said second machine language instruction(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).

As per claim 47, Tsushima taught wherein said modifying substitutes a bit pattern of a subset of said instruction segment (e.g., see col. 13, lines 23-66).

As per claim 48 Tsushima taught repeating fetching, said modifying and said executing without executing and intervening machine language instruction to change an instruction modification information value utilized by said modifying (e.g., see col. 13,

line 49-col. 14 line15)[the operation of fetching is continuously performed and the instruction are placed in a queue while the sub-instructions of a previous instruction is are being with same expanded with same group code and executed]. .

As per claim 49, Tsushima taught wherein said executing comprises executing microcode (e.g., see figs.1, 2A-2D and col. 5, lines 45-56).

As per claim 50, Tsushima taught said trigger pattern is associated with a particular execution unit of said processor (e.g., see figs 2C, 2D).

As per claim 51, Tsushima taught said first machine language instruction comprises a very long instruction word (e.g., see col. 5, lines 45-51).

As per claim 52, Tsushima taught wherein said instruction segment comprises an atomic portion of said very long instruction word (group code in fig. 2C and col. 8, lines 16-50).

As per claim 53 Tsushima taught a method of executing a processor instruction said method comprising fetching from memory a first machine language instruction comprising an instruction segment(e.g., see col. 6, lines 1-9); responsive to a trigger pattern in said first machine language instruction (group code fields 10A,16 in figs. 2C and 2D), accessing instruction modification information from a memory(instruction table memory 307 or main memory in fig. 4)(e.g., see col. 14, lines 16-65 and col. 22, lines 33-63); modifying said instruction segment according to said instruction modification information and information associated with said trigger pattern to form a second machine language instruction; executing on said processor said machine language instruction(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56); and wherein

said memory comprises a plurality of entries, each entry storing instruction modification information (e.g., see fig. 4 and col., 22, lines 53-63 and col. 8,lines 40-50).

As per claim 61 Tsushima taught a computer system (e.g., see fig. 1) comprising a memory(100, 307) for storing a first machine language instruction (e.g., see figs. 1,4); a second memory for storing a plurality of instruction modification information(808); a processor (200) coupled to said memory for executing machine language instructions; said processor also for implementing a method, said method comprising: fetching from said memory(202) said first machine language instruction comprising an instruction segment from said memory; responsive to a trigger pattern in said first machine language instruction(group code fields 10A,16 in figs. 2C and 2D), modifying said instruction segment using said instruction modification information to form a second machine language instruction and executing said processor second machine language instruction(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).

As to claim 62 Tsushima taught as cache for caching said first machine language instruction (e.g., see fig. 1)(VLIW instruction is stored in cache 201)(e.g., see col. 6, lines 1-9).

As to claim 63 Tsushima taught wherein said processor pipelines instruction execution (e.g., see fig. 1).

As to claim 66 taught a memory stored packed containing within a very long instruction word the packet (e.g., see fig. 1,2A,2B.2C,2D) comprising: a trigger pattern to initiate a modification of a segment of said very long instruction word(group code fields 10A,16 in figs. 2C and 2D); a first field to indicate a portion of said segment to be

modified a bit to indicate that a queue of instruction modification data is to be advanced in association with modification of said segment to be modified a and a second field to indicate how to modify said portion of said segment (e.g., see figs. 1,2A,2B,2C, 2D).[as to the particulars of the claimed packet, the VLIW instruction of Tsushima comprises bits which are memory stored for controlling a processor to perform operations and trigger the expansion of field of the instruction. The structure and function of the memory stored packet are met by the VLIW instruction of Tsushima to the extent claimed. Note that the features attributed to the packet are not performed or executed in the claimed invention and therefore the VLIW instruction portions provide equivalent structure and function to the claimed packet].

As to claim 67 Tsushima taught wherein said second field indicates a number of bits of instruction modification information to be substituted into said segment to be modified (e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).

As to claim 68 Tsushima taught wherein said second field operable to indicate substitution of a single bit into said segment to be modified(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).

As to claim 69 Tsushima taught wherein said trigger pattern identifies said segment according to a type of said segment (e.g., see fig. 1 and col. 8, lines 5-39).

As to claim 70 Tsushima taught wherein the trigger pattern identifies an arithmetic logic unit segment (e.g., see fig. 1 (e.g., see col. 8, lines 5-39).

As to claim 71 Tsushima taught wherein said trigger pattern identifies a floating point unit segment(205-1)(e.g., see fig. 1 and col. 8, lines 5-39).

As to claim 72 Tsushima taught wherein said trigger pattern identifies a memory unit segment(204-1,204-2) (e.g., see fig. 1)(e.g., see col. 8, lines 8-39).

As to claim 73 Tsushima taught said trigger pattern identifies a branch unit segment (e.g., see fig. 1)(e.g., see col. 8,lines 51-57).

As to claim 74 Tsushima taught said trigger pattern identifies said segment according to a position of said segment in said very long instruction word (e.g., see col. 5, lines 45-56).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 54-60, 64,65, 75-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tusushima (patent No. 6,044,450).

As per claim 54, Tsushima did not expressly detail comprising advancing a queue structure to a next entry storing instruction modification information in said memory. Tsushima however taught (e.g. see fig. 4) the table provides entry at one address location and exit at another address location namely the lower end of the table and therefore using the table of Tsushima one of ordinary skill would have been motivated to operate the table as at least one queue for access of opcode data. Also since the codes that accessed the table were queued one of ordinary skill would have been motivated to operate the table as a queue.

As per claim 55 Tsushima taught wherein said advancing comprises advancing a pointer to indicate said next entry storing instruction modification information in said memory(e.g., see col. 8,lines 40-50)[the queued group code provide pointers for the memory and so the advancing of the pointer is provided with the use of subsequent group codes].

As per claim 56 Tsushima taught comprising repeating said fetching, accessing modifying and executing without executing an intervening machine language to change any plurality of instruction modification information(e.g., see col. 13, line 49-col. 14 line15)[the operation of fetching is continuously performed and the instruction are placed in a queue while the sub-instructions of a previous instruction is are being with same expanded with same group code and executed]. .

As per claim 57 Tsushima taught wherein said executing comprises executing microcode (e.g., see figs.1, 2A-2D and col. 5, lines 45-56).

As per claim 58, Tsushima taught wherein said trigger pattern is associated with a particular execution unit of said processor e.g., see figs 2C, 2D).

As per claim 59 Tsushima taught wherein said first machine language instruction comprises a very long instruction word that comprises a plurality of instruction segments (e.g., see col. 5, lines 45-51 and figs. 2A,2B, 2C, 2D,11)

As per claim 60 Tsushima taught wherein said instruction segment comprises an atomic portion of said very long instruction word (fixed calculation portion)(e.g., see fig. 11).

As to claim 64 Tsushima did not expressly detail wherein said second memory comprises a queue. . Tsushima however taught (e.g. see fig. 4) the instruction table memory provides entry at one address location and exit at another address location namely the lower end of the table and therefore using the table of Tsushima one of ordinary skill would have been motivated to operate the table as at least one queue for access of opcode data. Also since the codes that accessed the table were queued one of ordinary skill would have been motivated to operate the table as a queue.

As to claim 65 Tsushima taught wherein said modifying comprises accesses an instruction modification information from said second memory and modifying said instruction segment according to said instruction modification information associated with said trigger pattern to form said second machine language instruction(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).

As to claim 75 Tushsima taught a method of modifying a machine language instruction, said method comprising, accessing said machine language instruction from memory(e.g., see col. 6, lines 1-9); recognizing a trigger pattern in said machine language instruction(group code fields 10A,16 in figs. 2C and 2D); Identifying a portion of said machine language instruction from a second memory of instruction modifications to form a second machine language instruction(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).

Tsushima did not expressly detail wherein said second memory comprises a queue. . Tsushima however taught (e.g. see fig. 4) the instruction table memory provides entry at one address location and exit at another address location namely the lower end of the table and therefore using the table of Tsushima one of ordinary skill would have been motivated to operate the table as at least one queue for access of opcode data. Also since the codes that accessed the table were queued one of ordinary skill would have been motivated to operate the table as a queue.

As to claim 76 Tsushima taught wherein said identifying comprises decoding said trigger pattern to identify said portion of said machine language instruction (e.g., see figs. 1, 2A, 2B, 2C, 2D).

As to claim 77 Tsushima taught wherein said portion of said machine language instruction is identified according to a type of said portion(e.g., see fig. 1 and col. 8, lines 5-39).

As to claim 78 Tsushima taught wherein said portion of said machine language instruction is identified according to a location of said portion within said machine language instruction(e.g., see fig. 1 and col. 8, lines 5-39).

As to claim 79 Tsushima taught a method of executing an instruction word of a processor (e.g., see fig. 1) comprising; accessing from a memory an instruction word comprising a plurality of instruction segments and a trigger portion(e.g., see col. 6, lines 1-9); based on said trigger portion(group code fields 10A,16 in figs. 2C and 2D), identifying a portion of information of a second memory for selection thereof; based on

said trigger portion, identifying a portion of one of said plurality of instruction segments; modifying said portion of said one of said plurality of instruction segments with said portion of information of said second memory ; and dispatching said one of said plurality of instruction segments, as modified by modifying to an execution unit of said processor(e.g., see col. 13, lines 23-66 and fig. 1 and col. 5, lines 45-56).
Tsushima did not expressly detail wherein said second memory comprises a queue. Tsushima however taught (e.g. see fig. 4) the instruction table memory provides entry at one address location and exit at another address location namely the lower end of the table and therefore using the table of Tsushima one of ordinary skill would have been motivated to operate the table as at least one queue for access of opcode data. Also since the codes that accessed the table were queued one of ordinary skill would have been motivated to operate the table as a queue.

As to claim 80 Tsushima taught wherein said instruction word is of a Very Long Instruction Word (VLIW) type(e.g., see col. 5,lines 45-56).

As to claim 81 Tsushima did not expressly detail taught advancing a position of said memory queue response to a bit field of said trigger position however since the access to a next non-compressed opcode occurred upon use of a group code pointing to at next non compress opcode then it would have been obvious to one of ordinary skill that the advancing of the position of the instruction table that is configured to operate as a queue. (e.g., see col. 8, lines 40-50)[the queued group code provide

pointers for the memory and so the advancing of the pointer is provided with the use of subsequent group codes].

As to claim 82 Tsushima taught wherein said trigger portion and said one of said plurality of instruction segments are both specific to said execution unit (e.g., see col. 8, lines 8-39)

As to claim 83 Tsushima taught wherein said execution unit is a memory execution unit (204-1,204-2) (e.g., see fig. 1)(e.g., see col. 8, lines 8-39).

As to claim 84 Tsushima taught wherein said execution unit is a arithmetic logic unit (ALU) (e.g., see fig. 1 (e.g., see col. 8, lines 5-39)).

As to claim 85, Tsushima taught wherein said execution unit is a floating point unit (FPU) (205-1)(e.g., see fig. 1 and col. 8, lines 5-39).

As to claim 86 Tsushima taught wherein said execution unit is a branch unit (207) (e.g., see fig. 1).

As to claim 87 Tsushima taught wherein said identifying and said modifying are performed by microcode internal to said processor (e.g., see col. 13, lines 1-67 and fig.1).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Denman (patent No. 5,784,585) disclosed a computer system for executing instruction stream containing mixed compressed and uncompressed instructions (e.g., see abstract).

Worrell (patent No. 5,867,681) disclosed a microprocessor having register dependent immediate decompression (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

/Eric Coleman/
Primary Examiner, Art Unit 2183